WE CLAIM:

1. A method for reducing leakage current across a circuit component, the circuit component comprising a first terminal and a second terminal, the method comprising:

electrically coupling the first terminal to a first voltage source, and

electrically coupling the second terminal to a second voltage source,

wherein the first voltage source provides a first voltage level and the second voltage source provides a second voltage level substantially equivalent to the first voltage level.

2. The method of claim 1, further comprising placing the circuit component into a standby mode.

3. The method of claim 1, wherein electrically coupling the second terminal comprises reconfiguring an electrical coupling to the second terminal.

4. The method of claim 1, wherein the second voltage source is the first voltage source.

5. The method of claim 1, wherein the first voltage level comprises a CMOS high voltage level.

6. The method of claim 1, wherein the first voltage level comprises a CMOS low voltage level.

7. The method of claim 1, wherein the circuit component comprises a MOS device.

8. The method of claim 7, wherein the MOS device comprises a transistor in a CMOS circuit.

9. A method of reducing leakage current in a circuit, the circuit comprising a circuit component comprising a first terminal and a second terminal, and a first voltage source, the method comprising:

electrically coupling the first voltage source to the first terminal, and

electrically coupling the first voltage source to the second terminal.

10. The method of claim 9, further comprising placing the circuit into a standby mode.

11. The method of claim 9, wherein electrically coupling the first voltage source to the second terminal comprises reconfiguring the circuit.

12. The method of claim 9, wherein the circuit comprises a barrel shifter, and the first circuit component comprises a pass device.

13. The method of claim 12, wherein the pass device comprises a pass transistor.

14. The method of claim 12, wherein the pass device comprises a pass gate.

15. The method of claim 9, wherein the circuit component comprises a bus switch coupling a source bus to a destination bus, and the first voltage source is coupled to both the source and destination busses.

16. The method of claim 9, wherein the circuit further comprises a second circuit component comprising an output, the output coupled to the first terminal, and wherein coupling

the first voltage source to the first terminal comprises coupling the first voltage source to the output of the second circuit component.

17. The method of claim 16, wherein the second circuit component further comprises a data input, and coupling the first voltage source to the output of the second circuit component comprises providing a signal to the data input, the signal causing the first voltage source to be coupled to the output of the second circuit component.

18. The method of claim 16, wherein the second circuit component further comprises a test input, and coupling the first voltage source to the output of the second circuit component comprises providing a signal to the test input, the signal causing the first voltage source to be coupled to the output of the second circuit component.

19. The method of claim 16, wherein the second circuit component further comprises a reset input, and coupling the first voltage source to the output of the second circuit component comprises providing a signal to the reset input, the signal causing the first voltage source to be coupled to the output of the second circuit component.

20. The method of claim 19, wherein the second circuit component comprises a register.

21. The method of claim 16, wherein the second circuit component further comprises a configuration input, and coupling the first voltage source to the output of the second circuit component comprises providing a signal to the configuration input, the signal causing the first voltage source to be coupled to the output of the second circuit component.

22. The method of claim 21, wherein the second circuit component comprises a register.

23. The method of claim 16, wherein the second circuit component comprises a register.

24. The method of claim 16, wherein the second circuit component comprises a driver.

25. A circuit, comprising:

a data input,

a data output,

a first voltage supply input,

a second voltage supply input,

a high threshold device electrically coupled between the data input and the data output, and electrically coupled between the first and second voltage supply inputs, and

a low threshold device electrically coupled between the data input and the data output, and electrically coupled between the first and second voltage supply inputs;

wherein the circuit is adapted to be switched to a low leakage state by providing a signal on the data input that causes the circuit to enter the low leakage state.

26. The circuit of claim 25, wherein the low leakage state comprises a leakage current path from the first voltage supply input to the second voltage supply input, the leakage current path flowing through the high threshold device, the high threshold device being turned off.

27. The circuit of claim 25, wherein the low leakage state comprises a standby mode for the circuit.

28. The circuit of claim 25, wherein the first voltage supply input comprises a CMOS high voltage supply input.

29. The circuit of claim 25, wherein the second voltage supply input comprises a CMOS low voltage supply input.

30. The circuit of claim 25, wherein the high threshold device comprises a MOS device.

31. The circuit of claim 30, wherein the MOS device comprises a transistor.

32. The circuit of claim 25, wherein the low threshold device comprises a MOS device.

33. The circuit of claim 32, wherein the MOS device comprises a transistor.

34. The circuit of claim 25, further comprising a second data input, a second high threshold device electrically coupled between the second data input and the data output, and electrically coupled between the first and second voltage supply inputs, and a second low threshold device electrically coupled between the second data input and the data output, and electrically coupled between the first and second voltage supply inputs, wherein the circuit is adapted to be switched to a low leakage state by providing a second signal on the second data input which in combination with the signal on the first data input causes the circuit to enter the low leakage state.

35. The circuit of claim 25, wherein the circuit comprises a controlled buffer.

36. The circuit of claim 25, wherein the circuit comprises a driver circuit.

37. The circuit of claim 25, further comprising a first register electrically coupled to the data input, the register comprising a test input, wherein the first register is adapted to provide the signal on the data input, and wherein the first register is adapted to receive a signal on the test input, and propagate that signal to the data input.

38. The circuit of claim 37, wherein the first register is one of a plurality of registers coupled together by a scan chain, the scan chain adapted to receive a series of data values and to load the series of data values into the plurality of registers.

39. The circuit of claim 38, wherein the circuit is adapted to be placed into a low leakage state by supplying a pre-determined series of data values to the scan chain, loading the predetermined series of data values into the plurality of registers, causing the first register to propagate one of the pre-determined data values to the data input, and causing the circuit to enter the low leakage state.

40. The circuit of claim 25, wherein the circuit comprises an integrated circuit.

41. A reconfigurable device comprising:

a plurality of processing devices, each comprising a processing device input and a processing device output;

a configurable routing network adapted to couple at least one of the processing device outputs with at least one of the processing device inputs, the configurable routing network comprising a plurality of low threshold devices;

wherein the reconfigurable device is adapted to be placed into a low leakage state that substantially prevents a leakage current from flowing across the low threshold devices.

42. The reconfigurable device of claim 41, wherein the configurable routing network comprises a plurality of pass transistors.

43. The reconfigurable device of claim 41, wherein the configurable routing network comprises a plurality of complementary switches.

44. The reconfigurable device of claim 41, wherein the configurable routing network comprises a plurality of controlled buffers.

45. The reconfigurable device of claim 41, wherein the configurable routing network comprises a plurality of multiplexers.

46. The reconfigurable device of claim 41, wherein the low leakage state comprises an equipotential drive condition.

47. The reconfigurable device of claim 46, wherein the reconfigurable device further comprises one or more data inputs electrically coupled to the plurality of processing devices, and the equipotential drive condition is created by applying a data sequence to the one or more data inputs.

48. The reconfigurable device of claim 47, wherein the data sequence causes the plurality of processing devices to present a plurality of output signals each having the same value to the routing network.

49. The reconfigurable device of claim 46, wherein the reconfigurable device is adapted to be reconfigured into a dedicated low leakage configuration, the low leakage configuration causing the equipotential drive condition.

50. The reconfigurable device of claim 49, wherein the dedicated low leakage configuration comprises a condition wherein the plurality of processing devices each output the same output value.

51. The reconfigurable device of claim 49, further comprising a plurality of registers, each register electrically coupled between an output of one of the plurality of processing devices and the configurable routing network, and wherein the dedicated low leakage configuration comprises a condition wherein the plurality of registers each output the same output value.

52. The reconfigurable device of claim 51, wherein the plurality of registers are adapted to preserve an application state configured into the plurality of registers, before the plurality of registers are placed into the low leakage configuration.

53. The reconfigurable device of claim 46, wherein the reconfigurable device is adapted to enter the low leakage state by undergoing a partial reconfiguration.

54. The reconfigurable device of claim 53, further comprising comprises a plurality of registers, each register electrically coupled between an output of one of the plurality of processing devices and the configurable routing network, wherein the partial reconfiguration comprises causing the plurality of registers to all output signals having the same value, while preserving a prior configuration of the plurality of processing devices.

55. The reconfigurable device of claim 53, further comprising comprises a plurality of registers, each register electrically coupled between an output of one of the plurality of processing devices and the reconfigurable routing network, wherein the partial reconfiguration comprises causing the plurality of registers to all output signals having the same value, while preserving a prior configuration of the configurable routing network.

56. The reconfigurable device of claim 53, wherein the partial reconfiguration comprises uncoupling one or more inputs to the configurable routing network, the one or more inputs comprising inputs that are not receiving an equipotential value, the equipotential value comprising a value that causes the equipotential drive condition.

57. The reconfigurable device of claim 56, wherein the uncoupled inputs are recoupled to a signal source, the signal source supplying the equipotential value.

58. The reconfigurable device of claim 46, further comprising a plurality of registers, each register electrically coupled between an output of one of the plurality of processing devices and the configurable routing network, wherein the reconfigurable device is adapted to enter a global reset state, the global reset state causing the plurality of registers to all enter a known state, the known state causing the plurality of registers to all output signals having the same value.

59. The reconfigurable device of claim 58, wherein the known state is a CMOS low signal state.

60. The reconfigurable device of claim 58, wherein the known state is a CMOS high signal state.

61. The reconfigurable device of claim 58, wherein the known state is a logical high signal state.

62. The reconfigurable device of claim 58, wherein the known state is a logical low signal state.

63. The reconfigurable device of claim 46, further comprising a plurality of registers, each register electrically coupled between an output of one of the plurality of processing devices and the configurable routing network, the plurality of registers each comprising a register content value and a standby mode input adapted to receive a standby mode signal, the plurality of registers adapted to output an equipotential value when the plurality of registers receives the standby mode signal, the plurality of registers adapted to preserve the register content value upon receipt of the standby mode signal.

64. The reconfigurable device of claim 41, wherein one or more of the plurality of processing devices comprises a logic gate coupled to the routing network, the logic gate comprising one or more inputs, wherein the logic gate is adapted to enter a low-leakage state when pre-selected values are placed on the one or more inputs.

65. The reconfigurable device of claim 64, wherein the pre-selected values comprises standby mode values, the standby mode values being placed on the one or more inputs when the reconfigurable device is placed into a standby mode.

66. The reconfigurable device of claim 64, wherein the logic gate comprises a CMOS logic gate comprising a PMOS device, an NMOS device, a PMOS current path through the PMOS device, and an NMOS current path through the NMOS device, wherein the logic gate is

adapted to turn off one of the PMOS device or the NMOS device when the one or more pre-selected values are placed on the one or more inputs, wherein the logic gate is adapted to turn on the other of the PMOS device and the NMOS device when the one or more pre-selected values are placed on the one or more inputs, wherein the device turned off comprises a high-threshold device, and wherein the device turned on comprises a low-threshold device.

67. The reconfigurable device of claim 41, wherein the processing devices comprise functional units.

68. The reconfigurable device of claim 41, wherein the processing devices comprise special purpose blocks.

69. The reconfigurable device of claim 41, wherein the processing devices comprise registers.

70. A method of placing a circuit into a standby state, the circuit comprising a memory and a plurality of registers, the registers each having a register value, the method comprising:

reading the plurality of register values out of the plurality of registers,

saving the plurality of register values into the memory, and

loading a plurality of standby values into the plurality of registers;

wherein the plurality of standby values are adapted to place the circuit into the standby state.

71. The method of claim 70, further comprising reading the saved plurality of register values out of the memory, and loading the saved plurality of register values into the plurality of registers.

72. The method of claim 71, wherein the saved plurality of register values are loaded into the plurality of registers using a scan chain.

73. The method of claim 71, wherein the saved plurality of register values are loaded into the plurality of registers using a configuration port.

The method of claim 70, wherein the plurality of register values are read out of the plurality of registers using a scan chain.

74. The method of claim 70, wherein the plurality of register values are read out of the plurality of registers using a configuration port.

75. The method of claim 70, wherein the standby state comprises a low leakage state.

76. The method of claim 75, wherein the plurality of standby values are determined by selecting a plurality of input values which when applied to the circuit result in a substantially minimized total aggregate leakage current in the circuit.

77. The method of claim 76, wherein the circuit comprises a plurality of circuit components each comprising one or more component inputs, and the plurality of input values are applied to the one or more component inputs.

78. A circuit, comprising:

a data input,

a data output,

a low threshold device electrically coupled between the data input and the data output, and electrically coupled to the control input,

a control input adapted to receive a control signal for controlling the low threshold device,and

a register electrically coupled between the data input and the low threshold device, the register adapted to provide a register value to the low threshold device;

wherein the circuit is adapted to be placed into a low leakage state by causing the register value to be a low leakage value, which causes the circuit to enter the low leakage state.

79. The circuit of claim 78, wherein the data output comprises a data output value of a first voltage level, and the low leakage value comprises a second voltage level substantially equivalent to the first voltage level.

80. The circuit of claim 78, wherein the register value is caused to be a low leakage value by providing the low leakage value as an input on the data input.

81. The circuit of claim 78, wherein the register further comprises a configuration input, and the register value is caused to be a low leakage value by providing the low leakage value as an input on the configuration input.

82. The circuit of claim 78, wherein the register further comprises a reset input, and the register value is caused to be a low leakage value by providing a reset signal to the reset input.

83. The circuit of claim 78, wherein the register further comprises a test input, and the register value is caused to be a low leakage value by providing the low leakage value as an input on the test input.

84. The circuit of claim 83, wherein the register is one of a plurality of registers, the plurality of registers coupled together by a scan chain, the scan chain adapted to receive a series of data values and to load the series of data values into the plurality of registers.

85. The circuit of claim 84, wherein the circuit is adapted to be placed into a low leakage state by supplying a pre-determined series of data values to the scan chain, loading the predetermined series of data values into the plurality of registers, causing the first register to propagate one of the pre-determined data values as the register value to the low threshold device, and causing the circuit to enter the low leakage state.